



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,893	02/11/2002	Takuya Kitamura	8022-1003	3547

466 7590 02/10/2003

YOUNG & THOMPSON
745 SOUTH 23RD STREET 2ND FLOOR
ARLINGTON, VA 22202

EXAMINER

FOONG, SUK SAN

ART UNIT PAPER NUMBER

2823

DATE MAILED: 02/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/068,893

Applicant(s)

KITAMURA, TAKUYA

Examiner

Suk-San Foong

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 2/11/02 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II, claims 1-13, in Paper No. 7 is acknowledged.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "16" has been used to designate both inter-level dielectric and bottom electrode in Fig. 4. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: instant page 21, line 3, and other occurrences, it appears that "oxinitride" should be replaced by--oxynitride--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Art Unit: 2823

5. Claims 3-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites the limitation "said contact barrier layer" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in combination with Diodato et al. ('522).

AAPA discloses a memory cell array for DRAM which includes a substrate 100 (instant Fig. 1), MOS transistors formed in a surface portion of substrate 100 wherein the MOS transistors includes source region 113, drain region 114 and gate 103 (instant p. 1, line 26 to instant p. 2, line 1), first inter-level dielectric 116 covering MOS transistors (instant p. 2, lines 16-18), capacitor element includes bottom electrode 106, dielectric layer 107 formed on bottom electrode 106 and upper electrode 108/109 (instant p. 2, line 26 to p. 3, line 3), first contact 104 formed through first inter-level dielectric 116 to electrically connect source 113 to bottom

Art Unit: 2823

electrode 106 (instant p. 3, lines 3-4), second inter-level dielectric 122 over first inter-level dielectric layer 116, and third inter-level dielectric 135 over first inter-level dielectric 116 and capacitor element (instant p. 3, lines 11-15), plug 102 formed through first inter-level dielectric 116 and second inter-level dielectric 122 to electrically connect to drain 114 (instant p. 3, lines 16-19), and bit line 103 formed on third inter-level dielectric 116 (instant p. 3, lines 16-19).

AAPA does not disclose that contact formed in the first inter-level dielectric is comprised of a first metal portion comprised of tungsten and barrier layer comprised of titanium nitride between source and first metal portion.

Diodata et al. discloses a DRAM device which includes a peripheral circuit region 34 and memory region 36 (Paragraph [0021], and Figs. 1A and 1B) wherein transistors 16 and 18 are formed on both surfaces in both regions 34 and 36 (Paragraphs [0019, 0039]), first inter-level dielectric 14 formed over both regions 34 and 36 (Paragraphs [0039] and Figs. 1A and 5), first contact 32 over region 62, comprised of source 47 or drain 48 of transistor 16, formed through first inter-level dielectric 14 which includes barrier layer 64 such as titanium nitride and refractory metal such as tungsten thereby electrically connecting to bottom electrode 42 of capacitor element 20 (Paragraphs [0040-0042] and Figs. 7-8), capacitor element 20 (Paragraph [0046] and Fig. 9), fourth contact 31 through first inter-level dielectric 14 to connect source/drain region of transistor 18 (Paragraph [0020] and Figs 1A and 1B), fifth contact 25 connected to fourth contact 31 which includes a third metal portion 25.

It would have been within the scope to one ordinary skill in the art to combine the teachings of APPA with Diodato et al. because it would enable formation first contact 104 of APPA to be performed.

8. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in combination with Diodato et al. ('522) as applied to claims 1-3 as previously applied, and further in view of Parekh et al. ('380)

The combination does not disclose formation of a second contact and a third contact through first inter-level dielectric and second inter-level dielectric.

Parekh et al. discloses a DRAM device which includes a memory array region 12 with MOS transistors and peripheral regions 14 and 16 with MOS transistors (Paragraphs [0021, 0023] and Fig. 1), first and second contacts 52 and fourth contacts 54 and 56 through first inter-level dielectric 20 connected to source/drain regions 40, 42 and 44 (Paragraph [0024]), second inter-level dielectric 22 (Paragraph [0027]), third contact 86 formed through second inter-level dielectric 22 in the memory array region 12 thereby electrically contacting second contact 52 (Fig. 4B), fifth contact 86 formed through second inter-level dielectric 22 in the peripheral region 16 thereby electrically contacting fourth contacts 54 and 56 which includes a third portion 90 (Fig. 4B), and capacitor elements 78 (Fig. 5B).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Parekh et al. with the combination to employ second contact 52 and third contact 86 in the memory array region 12 of Parekh et al. for formation of plug 102 of the combination to be performed and obtain further advantage of facilitating formation of contacts and enhancing local interconnect contact formation (Parekh et al., Paragraph [0006]).

With respect to claim 9, the combination does not disclose the step as recited.

In view of the disclosure of Diodato et al. of the peripheral circuit region, it would have been within the scope to one ordinary skill in the art to combine both the teachings because it would enable formation of the DRAM device of the combination to be performed.

9. Claims 4, 5, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in combination with Diodato et al. ('522) as applied to claims 1-3 above, and further in view of Amico et al. ('498).

The combination fails to disclose that the bottom electrode includes an electrode barrier layer formed between first metal portion and polysilicon layer.

Amico et al. discloses a capacitor in semiconductor devices which includes first contact 14 comprised of material such as tungsten (Paragraph [0024] and Fig. 1), and a bottom electrode including polysilicon layer 20, electrode barrier layer 18 comprised titanium nitride formed between first contact 14 and polysilicon layer 20 (Paragraph [0025] and Fig. 2) and dielectric layer 24 (Paragraph [0029] and Fig. 7).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Amico et al. with the combination because it would enable formation of the capacitor element the combination to be performed and obtain further advantage of increasing the throughput during manufacturing of semiconductor devices (Amico et al., Paragraph [0033]).

10. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in combination with Diodato et al. ('522) and Amico et al. ('498) as applied to claims 1-3, and 4, 5, 10 and 11 above, and further in view of Fukuda et al. ('526).

The combination does not disclose the step as recited in claim 12.

Fukuda et al. discloses a DRAM device which includes at least one transistor including gate electrode 20 and source/drain regions 24 and 26 (Paragraph [0124] and Figs. 8, 19 and 20A), first contact 38 (Paragraph [0125]), a capacitor element including electrode barrier layer 74 comprised of material that enhances physical, electric adhesion and barrier properties between layers (Paragraph [0054]) and bottom electrode portion 76 comprised of polysilicon (Paragraph [0107]) and dielectric layer 78 comprised of material such as Ta₂O₅ (Paragraph [0135] and Fig. 21B), and second dielectric layer 70. Furthermore, the end portions of the side of electrode barrier layer 74 is out of alignment with upper surface of second dielectric layer 70 thereby not reaching the upper surface of second dielectric layer 70 (Figs. 7A and Fig. 20B). And the end of the side bottom electrode portion 76 is in alignment with upper surface of second inter-level dielectric layer 70 (Figs. 7B, 20B, 21A-21B).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Fukuda et al. with the combination because it would enable formation of the capacitor element of the combination to be performed and obtain further advantage of mitigating electric field concentrations on the upper ends of bottom electrodes and preventing leakage current increase and dielectric breakdown of the capacitor dielectric film (Fukuda et al., Paragraph [0022]).

Conclusion


11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.


Art Unit: 2823

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suk-San Foong whose telephone number is 703-305-0383. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 (7724, 3431, 3432).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.


February 5, 2003


George Fourson
Primary Examiner
Art Unit 2823